Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **VOUT**
2. **ADJ**
3. **VOUT**
4. **VIN (x2 wire)**
5. **VOUT**
6. **NC**
7. **NC**
8. **NC**
9. **NC**

**.064”**

**.073”**

**9 8 7 6**

**4**

**1**

**2**

**5**

**3**

**317S**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: TiNiAg**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VOUT**

**Mask Ref: 317S**

**APPROVED BY: DK DIE SIZE .064” X .073” DATE: 8/15/23**

**MFG: SILICON SUPPLIES THICKNESS .014” P/N: LM117KG-MD8**

**DG 10.1.2**

#### Rev B, 7/1